

Reply to Office Action dated September 28, 2005

**REMARKS**

Claims 1-4, 6-20 and 22-34 are pending in this application. By this Amendment, claims 1, 18, 22 and 30 are amended and claims 5 and 21 are canceled without prejudice or disclaimer.

Entry of these amendments is proper under 37 C.F.R. §1.116 because the amendment: a) place the application in condition for allowance for the reasons set forth below; b) do not raise any new reasons that require further search and/or consideration; and c) place the application in better form for an appeal should an appeal be necessary. More specifically, independent claim 1 is amended to include features of dependent claim 5 and independent claim 18 is amended to include features of dependent claim 21. Thus, no new issues are raised. Entry is therefore proper under 37 C.F.R. §1.116.

The Office Action rejects claims 1-34 under 35 U.S.C. §102(b) by U.S. Patent 4,567,577 to Oliver. The rejection is respectfully traversed with respect to the pending claims.

Independent claim 1 recites a first transistor pair coupled between a supply voltage line and GROUND, and a second transistor pair coupled between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage based on a first mode of the memory device and to receive a second supply voltage based on a second mode of the memory device, the second supply voltage being different than the first supply voltage. Independent claim 1 also recites a bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a non-ACTIVE mode/state.

Reply to Office Action dated September 28, 2005

Oliver does not teach or suggest all these features of independent claim 1. In particular, the Office Action asserts that Oliver's transistor 35 corresponds to the claimed bias transistor and that the transistor 35 has a source connected to ground VSS. However, Oliver shows that when the WRITE line is inactive, then the transistor 35 has its gate activated. This results in a voltage of VSS being applied to bodies of transistors 25 and 27, "causing them to function as normal n-channel devices." Additionally, as shown in FIG. 2, each of transistors 25 and 27 are coupled to the voltage of VSS. Thus, when the WRITE line is inactive, a substantially same voltage (VSS) will be applied to transistors 25 and 27. This does not suggest to apply a forward body bias since the transistors are already being supplied with a supply voltage of VSS. Additionally, Oliver does not state that VSS is a ground voltage as alleged in the Office Action. At one point, Oliver states that VSS is a negative voltage. See Oliver's col. 3, line 8, for example.

Oliver does not teach or suggest a bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a non-ACTIVE mode/state. As stated above, when the WRITE line is inactive, a voltage of VSS is applied to bodies of transistors 25 and 27 and the voltage VSS is the supply voltage to the transistors 25 and 27. This does not relate to a forward body bias based on a non-ACTIVE mode/state.

Still further, independent claim 1 recites that the supply voltage line to receive a first supply voltage based on a first mode of the memory device and to receive a second supply voltage based on a second mode of the memory device, the second supply voltage being

Reply to Office Action dated September 28, 2005

different than the first supply voltage. Similar features were recited in previous dependent claim

5. These features are not addressed in the Office Action. Oliver does not teach or suggest these features of independent claim 1 as Oliver receives the same supply voltage VSS (for transistors 25 and 27) regardless of the alleged mode of the memory device. Stated differently, Oliver does not disclose that the supply voltage VSS changes based on a mode of a memory device.

The Office Action appears to state that the transistor 35 and its gate being activated when a WRITE signal being inactive inherently reads on the STANDBY signal. This is not true. As is well known in the art, a memory may have various states such as WRITE, READ and INACTIVE, for example. Thus, when a WRITE signal is inactive (as alleged in the Office Action), the memory may be in an inactive state or may be in an active state (such as a READ). Therefore the Office Action's assertion that an inactive WRITE signal inherently reads on a STANDBY signal is incorrect since the memory may be in an ACTIVE state (such as a READ).

The law of inherency states that:

To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Therefore, a WRITE signal being inactive may correspond to an ACTIVE state. Accordingly, applicants respectfully disagree with the Office Action's statement that a WRITE signal being inactive inherently reads on the STANDBY signal.

For at least the reasons set forth above, Oliver does not teach or suggest all the feature of independent claim 1. Thus, independent claim 1 defines patentable subject matter.

Independent claim 9 also defines patentable subject matter for at least similar reasons. That is, independent claim 9 recites a supply voltage line to provide a first supply voltage to two transistors of the first SRAM memory cell based on a first mode of the first SRAM memory cell and to provide a second supply voltage to the two transistors based on a second mode of the first SRAM memory cell, the second supply voltage being different than the first supply voltage.

Independent claim 9 also recites a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell.

Oliver does not teach or suggest providing a supply voltage to two transistors of a first SRAM memory cell based on a mode of a SRAM device. Rather, Oliver clearly shows supply voltage VSS being applied to transistors 25 and 27 (and the transistors 24 and 29 coupled to VDD). Further, there is no suggestion for the claimed first and second supply voltage. Accordingly, independent claim 9 defines patentable subject matter.

Independent claim 18 also defines patentable subject matter for at least similar reasons as set forth above. That is, independent claim 18 recites a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device. Independent claim 18 further recites the power control unit to apply a first voltage level in a first mode and to apply a second voltage level in a second mode. Independent claim 18 also recites the SRAM device including a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit

Reply to Office Action dated September 28, 2005

indicative of the mode. Oliver does not teach or suggest these features for at least similar reasons as set forth above. Additionally, the Office Action does not even address the claimed power control unit. Accordingly, independent claim 18 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 9 and 18 define patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references. For example, dependent claim 6 relates to a STANDBY signal. However, Oliver's WRITE signal being inactive does not necessarily correspond to a STANDBY signal indicative of a STANDBY state of a memory device. This is, the present application clearly describes a STANDBY signal and a STANDBY state of a memory device. For similar reasons as stated above, one skilled in the art would clearly know that Oliver's WRITE signal, or lack of WRITE signal, does not necessarily correspond to a STANDBY signal indicative of a STANDBY state of a memory device. Rather, Oliver's WRITE signal merely relates to whether data is being written. The lack of a WRITE signal does not necessarily correspond to a STANDBY state of a memory device. Thus, dependent claim 6 defines patentable subject matter at least for this additional reason.

Each of dependent claims 7, 14, 15, 22-29 and 31-34 also relate to a STANDBY mode. Oliver does not teach or suggest these features for at least the reasons set forth above. Thus, each of these dependent claims defines patentable subject matter at least for this additional reason.

Reply to Office Action dated September 28, 2005

Dependent claim 10 further recites a power control unit to change the supply voltage on the supply voltage line based on the mode of the first SRAM memory cell. Oliver does not teach or suggest a power control unit to change the supply voltage on the supply line based on the mode of the first SRAM memory cell. Rather, Oliver provides VSS to transistors 25 and 27 and provides VDD to transistors 24 and 29. Thus, dependent claim 10 defines patentable subject matter at least for this additional reason.

### **CONCLUSION**

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-4, 6-20 and 22-34 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

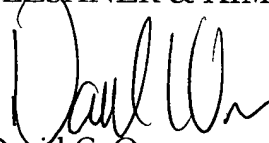
Serial No. **10/812,894**

Docket No. **INTEL-0056**

Reply to Office Action dated September 28, 2005

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,  
FLESHNER & KIM, LLP



David C. Oren  
Registration No. 38,694  
Attorney for Intel Corporation

P.O. Box 221200  
Chantilly, Virginia 20153-1200  
(703) 766-3701 DCO/kah

**Date: December 28, 2005**

**Please direct all correspondence to Customer Number 34610**